EXHIBIT 2

FCCM

Conference Dates: April 5-7, 2009
Submission Deadline: Jan 16, 2009
Location: Napa, CA

Field-Programmable Custom Computing Machines

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FCCM 2004

April 20-23, 2004
Napa Valley, California

Session 1: Architecture
Chair: Scott Hauck (University of Washington)

Time-Critical Software Deceleration in an FCCM
P. James-Roxby, G. Brebner, D. Bemmann (Xilinx and Humboldt University)

Design Patterns for Reconfigurable Computing
A. DeHon, J. Adams, M. DeLorimier, N. Kapre, Y. Matsuda, H. Naeimi, M. Vanier, M. Wrighton (Caltech)

Virtual Memory Window for Portable Reconfigurable Cryptography Coprocessor
M. Vuletic, L. Pozzi and P. Ienne (Swiss Federal Institute of Technology Lausanne)

Session 2: Tools I
Chair: Katherine Compton (University of Wisconsin)

Overview of the FREEDOM Compiler for Mapping DSP Software to FPGAs
G. Mittal, D. Zaretsky, X. Tang, P. Banerjee (Northwestern University)

PyGen: A MATLAB/Simulink based Tool for Parameterized and Energy

J. Ou and V. Prasanna (University of Southern California)

Session 3: Arithmetic I
Chair: Tom Kean (Algotronix)

Automated Least-Significant Bit Datapath Optimization for FPGAs
M.L. Chang and S. Hauck (University of Washington)

An Arithmetic Library and its Application to the N-body Problem
K.H. Tsoi, C.H. Ho, H.C. Yeung and P.H.W. Leong (Chinese University of Hong Kong)

Unifying Bit-width Optimisation for Fixed-point and Floating-point Designs
A. Gaffar, O. Mencer, W. Luk and P.Y.K. Cheung (Imperial College London)

Session 4: Communications Applications
Chair: Wayne Luk (Imperial College)

A Dynamically Reconfigurable, Power-Efficient Turbo Decoder
J. Liang, R. Tessier and D. Goeckel (University of Massachusetts)

A Flexible Hardware Encoder for Low-Density Parity-Check Codes
D-U Lee, W. Luk, C. Wang, C. Jones, M. Smith, J. Villasenor (Imperial College of Science Technology and Medicine)

Session 5: Networking I
Chair: Brad Hutchings (Tabula)

ShareStreams: A Scalable Architecture and Hardware Support for High-Speed QoS Packet Schedulers
R. Krishnamurthy, S. Yalamanchili, K. Schwan, R. West

(Georgia Tech)

Deep Packet Filter with Dedicated Logic and Read Only Memories
Y. Cho and W. Mangione-Smith (UCLA)

A Methodology for Synthesis of Efficient Intrusion Detection Systems on FPGAs
Z. Baker and V. Prasanna (University of Southern California)

Session 6: Applications I
Chair: Satnam Singh (Microsoft)

Smart Camera Based on Reconfigurable Hardware Enables Diverse Real-Time Applications
M. Leeser, S. Miller and H. Yu (Northeastern University)

FPGA-Based Acceleration of the 3D Finite-Difference Time-Domain Method
J. Durbano, F. Ortiz, J. Humphrey, P. Curt, D. Prather (EM Photonics and University of Delaware)

Session 7: Tools II
Chair: Mike Butts (Tabula)

Register Binding for FPGAs with Embedded Memory
H. Al Atat and I. Ouaiss (Lebanese American University)

Defect and Fault Tolerance for Reconfigurable Molecular Computing
M. Tahoori and S. Mitra (Northeastern Univ. and Intel)

Communications Scheduling for Concurrent Processes on Reconfigurable Computers
M. Gokhale, C. Ahrens, J. Frigo, C. Wolinski (Los Alamos National Lab)

Session 8: Applications II
Chair: Maya Gokhale (Los Alamos National Lab)

Reconfigurable Molecular Dynamics Simulator
N. Azizi, I. Kuon, A. Egier, A. Darabiha and P. Chow (University of Toronto)

Accelerating Seismic Migration Using FPGA-based Coprocessor Platform
C. He, M. Lu, C. Sun (Texas A&M University)

Session 9: Arithmetic II
Chair: Andre' DeHon (Caltech)

Closing the gap: CPU and FPGA Trends in Sustainable Floating-Point BLAS Performance
Keith D. Underwood and K. Scott Hemmert (Sandia National Labs)

FPGA-Based Implementation of a Robust IEEE-754 Exponential Unit
C. Doss and R. Riley (North Carolina A & T and AFRL)

On-Line IEEE Floating-Point Arithmetic for FPGAs
S. Krueger, P-M. Seidel (Texas Instruments and Southern Methodist University)

Session 10: Networking II
Chair: Jeffrey Arnold (Stretch)

Scalable Multi-Pattern Matching on High-Speed Networks
C. Clark and D. Schimmel (Georgia Institute of Technology, Atlanta, GA)

Pre-decoded CAMs for Efficient and High-Speed NIDS Pattern Matching
Ioannis Sourdis and Dionisios Pnevmatikatos (Technical University of Crete)